In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1. (Currently Amended) A method, comprising:

decoding an original instruction into a complementary-predicated pair of instructions by sending a hint to a register renaming circuit, the complementary-predicated pair of instructions including a predicate-positive instruction and a predicate-negative move instruction;

sequencing the predicate-positive instruction and the predicate-negative move instruction for out-of-order execution;

renaming, by the register renaming circuit, both a first destination register of the predicate-positive instruction and a second destination register of the predicate-negative move instruction to a same physical register, wherein the hint to permit the renaming to the same physical register; and

retiring either the predicate-positive instruction or the predicate-negative move instruction responsive to a predicate value associated with both instructions.

2. (Previously Presented) The method of claim 1, wherein the predicate-negative move instruction is responsive to a complement of the predicate value.

3. (Canceled)

4. (Currently Amended) The method of claim 1 [[3]], wherein the sending includes sending the hint via a trace cache.

5. (Canceled)

6. (Currently Amended) The method of claim 1 [[5]], further comprising squashing the predicate-negative move instruction when the predicate-positive instruction executes before the predicate-negative move instruction and the predicate value is true.

7. (Previously Presented) The method of claim 6, wherein the squashing occurs before the predicate-negative move instruction executes.

8. (Currently Amended) The method of claim 1 [[5]], further comprising squashing the predicate-positive instruction when the predicate-negative move instruction executes before the predicate-positive instruction and the predicate value is false.

9. (Previously Presented) The method of claim 8, wherein the squashing occurs before the predicate-positive instruction executes.

10. (Currently Amended) A processor, comprising:

a decode circuit to decode an original instruction into a complementary-predicated pair of instructions by sending a hint, the complementary-predicated pair of instructions including a predicate-positive instruction and a predicate-negative move instruction;

a sequencer to permit out-of-order execution of the predicate-positive instruction and the predicate-negative move instruction;

a register renaming circuit to receive the hint and, in response to the hint, to map a first destination register of the predicate-positive instruction to a physical register, and to map a second destination register of the predicate-negative move instruction to the same physical register, wherein the hint to permit the renaming to the same physical register; and

a retirement circuit to update the physical register with a result of either the predicate-positive instruction or the predicate-negative move instruction responsive to a predicate value associated with both instructions.

11. (Previously Presented) The processor of claim 10, wherein the predicate-negative move instruction is responsive to a complement of the predicate value.

12. (Canceled)

13. (Currently Amended) The processor of claim 10 [[12]], wherein the hint is sent via a trace cache.

14. (Canceled)

15. (Currently Amended) The processor of claim 10 [[14]], wherein the retirement circuit squashes the predicate-negative move instruction when the predicate-positive instruction executes before the predicate-negative move instruction and the predicate value is true.

16. (Currently Amended) The processor of claim 10 [[14]], wherein the retirement circuit squashes the predicate-positive instruction when the predicate-negative move instruction executes before the predicate-positive instruction and the predicate value is false.

17. (Currently Amended) The processor of claim 10 [[14]], further comprising execution units to execute the predicate-positive instruction and the predicate-negative move instruction in parallel.

18. (Currently Amended) A processor, comprising:

means for decoding an original instruction into a complementary-predicated pair of instructions by sending a hint to a register renaming circuit, the complementary-predicated pair of instructions including a predicate-positive instruction and a predicate-negative move instruction;

means for sequencing the predicate-positive instruction and the predicate-negative move instruction for out-of-order execution;

means for renaming, by the register renaming circuit, both a first destination register of the predicate-positive instruction and a second destination register of the predicate-negative move instruction to a same physical register, wherein the hint to permit the renaming to the same physical register; and

means for retiring either the predicate-positive instruction or the predicate-negative move instruction responsive to a predicate value associated with both instructions.

19. (Previously Presented) The processor of claim 18, wherein the predicate-negative move instruction is responsive to a complement of the predicate value.

20. (Canceled)

21. (Canceled)

22. (Currently Amended) The processor of claim 18 [[21]], further comprising means for squashing the predicate-negative move instruction when the predicate-positive instruction executes before the predicate-negative move instruction and the predicate value is true.

23. (Currently Amended) The processor of claim 18 [[21]], further comprising means for squashing the predicate-positive instruction when the predicate-negative move instruction executes before the predicate-positive instruction and the predicate value is false.

24. (Currently Amended) A system, comprising:

a processor, including:

a decode circuit to decode an original instruction into a complementary-predicated pair of instructions by sending a hint, the complementary-predicated pair of instructions including a predicate-positive instruction and a predicate-negative move instruction;

a sequencer to permit out-of-order execution of the predicate-positive instruction and the predicate-negative move instruction;

a register renaming circuit to receive the hint and, in response to the hint, to map a first destination register of the predicate-positive instruction to a physical register, and to map a second destination register of the predicate-negative move instruction to the same physical register, wherein the hint to permit the renaming to the same physical register; and

a retirement circuit to update the physical register with a result of either the predicate-positive instruction or the predicate-negative move instruction responsive to a predicate value associated with both instructions;

a bus to couple the processor to input/output devices; and

a communications device coupled to the bus.

25. (Previously Presented) The system of claim 24, wherein the predicate-negative move instruction is responsive to a complement of the predicate value.

26. (Canceled)

27. (Canceled)

28. (Currently Amended) The system of claim 24 [[27]], wherein the retirement circuit squashes the predicate-negative move instruction when the predicate-positive instruction executes before the predicate-negative move instruction and the predicate value is true.

29. (Currently Amended) The system of claim 24 [[27]], wherein the retirement circuit squashes the predicate-positive instruction when the predicate-negative move instruction executes before the predicate-positive instruction and the predicate value is false.